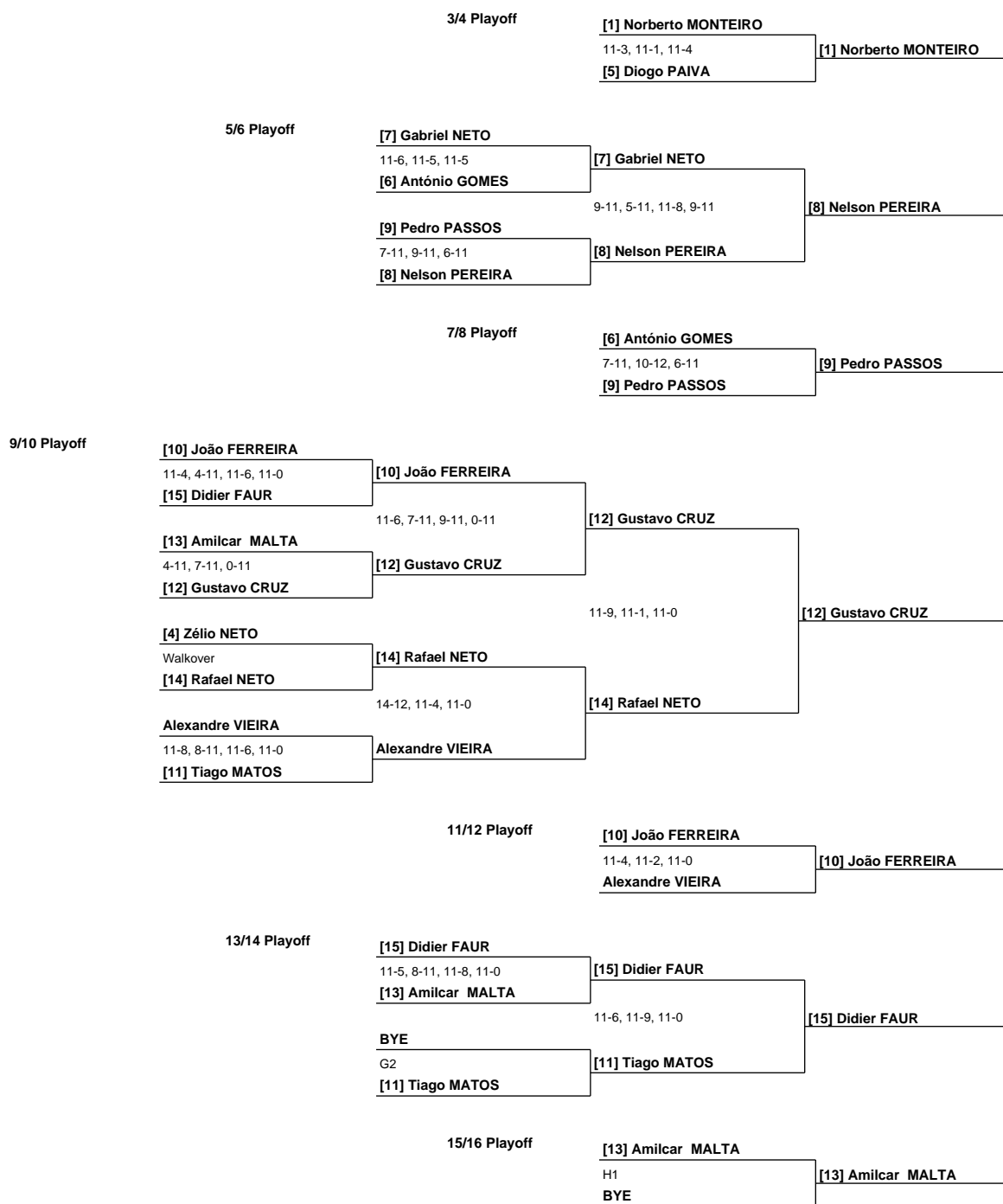


[illegible]



BYE					
I1	BYE				
BYE					
	I9	Pedro GOUVEIA			
Pedro GOUVEIA					
I2	Pedro GOUVEIA				
BYE					
		I13	Pedro GOUVEIA		
BYE					
I3	BYE				
BYE					
	I10	BYE			
BYE					
I4	BYE				
BYE					
			4-11, 5-11, 0-11	João Ferreira COIMBRA	
BYE					
I5	BYE				
BYE					
	I11	João Ferreira COIMBRA			
João Ferreira COIMBRA					
I6	João Ferreira COIMBRA				
BYE					
		Walkover	João Ferreira COIMBRA		
BYE					
I7	[16] José MONTEIRO				
[16] José MONTEIRO					
	I12	[16] José MONTEIRO			
BYE					
I8	BYE				
BYE					

BYE	
J1	
BYE	

The diagram illustrates a 4-bit bus system with two data buses, K2 and K3, and a common 'BYE' signal. The master's data bus (K3) is active for a longer duration than the slave's data bus (K2). The 'BYE' signal is active during the master's data transfer. The diagram shows the master sending data to the slave, with the master's data bus (K3) and the slave's data bus (K2) both showing a 'BYE' signal.

BYE	
L1	
BYE	

```

graph TD
    Root[BYE] --> M1[M1]
    Root --> M2[M2]
    M1 --> B1[BYE]
    M1 --> M5[M5]
    M2 --> B2[BYE]
    M2 --> M7[M7]
    M5 --> B3[BYE]
    M5 --> M6[M6]
    M7 --> B4[BYE]
    M7 --> M3[M3]
    M6 --> B5[BYE]
    M6 --> M4[M4]
    M3 --> B6[BYE]
    M3 --> M4
    M4 --> B7[BYE]
    M4 --> M4
  
```

27/28 Playoff

BYE

N1

BYE

29/30 Playoff

BYE

O1

BYE

BYE

O3

BYE

O2

BYE

BYE

31/32 Playoff

BYE

P1

BYE